University of Pune

COURSE STRUCTURE FOR M.E. (E & TC) (VLSI & Embedded Systems)
(w. e. f. June – 2013)

SEMESTER I

CODE	SUBJECT	TEACHING SCHEME	EXAMINATION SCHEME					CREDITS
		Lect./ Pr	Paper		TW	Oral/ Presentation	Total	
			In Semester Assessment	End Semester Assessment				
504201	Digital CMOS Design	4	50	50	-	-	100	4
504103	Embedded System Design	4	50	50	-	-	100	4
504203	Reconfigurable Computing	4	50	50	-	-	100	4
504104	Research Methodology	4	50	50	-	-	100	4
504205	Elective I	5	50	50	-	-	100	5
504206	Lab Practice I	4	-	-	50	50	100	4
Total		25	250	250	50	50	600	25

SEMESTER II

CODE	SUBJECT	TEACHING SCHEME	EXAMINATION SCHEME					CREDITS
		Lect./ Pr	Paper		TW	Oral/ Presentation	Total	
			In Semester Assessment	End Semester Assessment				
504207	Analog CMOS Design	4	50	50	-	-	100	4
504208	System on Chip	4	50	50	-	-	100	4
504209	Embedded Signal Processors	4	50	50	-	-	100	4
504210	Elective II	5	50	50	-	-	100	5
504211	Lab Practice II	4	-	-	50	50	100	4
504212	Seminar I	4	-	-	50	50	100	4
Total		25	200	200	100	100	600	25

SEMESTER III

CODE	SUBJECT	TEACHING SCHEME	EXAMINATION SCHEME					CREDITS
		Lect./ Pr	Paper		TW	Oral/ Presentation	Total	
			In Semester Assessment	End Semester Assessment				
604201	Fault Tolerant Systems	4	50	50	-	-	100	4
604202	ASIC Design	4	50	50	-	-	100	4
604103	Elective III	5	50	50	-	-	100	5
604204	Seminar II	4	-	-	50	50	100	4
604205	Project Stage I	08	-	-	50	50	100	8
Total		25	150	150	100	100	500	25

SEMESTER IV

CODE	SUBJECT	TEACHING SCHEME	EXAMINATION SCHEME				CREDITS
		Lect./ Pr	Paper	TW	Oral/ Presentation	Total	
604206	Seminar III	5	-	50	50	100	5
604207	Project Work Stage II	20	-	150	50	200	20
Total		25	-	200	100	300	25

Elective I	1. Mathematics for VLSI and Embedded Systems 2. Neural Networks In Embedded Applications 3. Processor Design 4. Wireless Sensor Network 5. *LATEX
Elective II	1. Embedded Product Design 2. VLSI Interconnections 3. Mixed Signal Circuit Design 4. Software Defined Radio 5. *Software Tools
Elective- III	1.Value Education, Human Rights and Legislative Procedures 2. Environmental Studies 3. Energy Studies 4. Disaster Management 5. Knowledge Management 6. Foreign Language 7. Economics for Engineers 8. Engineering Risk – Benefit Analysis 9. Technology Play 10. Optimization Techniques 11. Fuzzy Mathematics 12. Design and Analysis of Algorithms 13. CUDA

Note: Syllabus for Elective III is common for all discipline.

504201	Digital CMOS Design	
Teaching Scheme: Lectures 4 Hrs/ Week		**Examination scheme: Theory : 50 Marks (In Semester) 50 Marks (End Semester) Credits : 4**
Module I		
MOSFET Models and Layout MOS Capacitance models, MOS Gate Capacitance Model, MOS Diffusion Capacitance Model. Non ideal I-V Effects, MOSFET equivalent circuits and analysis, Parasitic; Technology scaling; Lambda parameter; wiring parasitic; SPICE Models, CMOS layout techniques; Transient response. CMOS Technologies: Layout Design Rules CMOS Process Enhancements: Transistors, Interconnect, Circuit Elements, Beyond Conventional CMOS. CMOS Fabrication and Layout: Inverter Cross-section, Fabrication Process, Stick Diagrams.		
Module II		
Performance parameters Static, dynamic and short circuit power dissipations; Propagation delay; Power delay product; Fan in, fan out and dependencies. Delay Estimation: RC Delay Models, Linear Delay Model, Logical Effort, Parasitic Delay. Logical Effort and Transistor Sizing: Delay in a Logic Gate, Delay in Multistage Logic Networks, Interconnect: Resistance, Capacitance, Delay, Crosstalk. Design Margin:		
Module III		
Logic design Static CMOS Logic : Inverter, NAND Gate, Combinational Logic, NOR Gate, Compound Gates, Pass Transistors and Transmission Gates, Tristates, Multiplexers, Latches and Flip-Flops, Design calculations for combinational logic and active area on chip; Hazards, sources and mitigation techniques, case study; HDL codes for FSM, Metastability and solutions; Transmission gate, utility and limitations		
Module IV		
Advanced trends Circuit Families: Static CMOS, Ratioed Circuits, Cascode Voltage Switch Logic, Dynamic Circuits, Domino logic; NORA logic, Differential Circuits, Sense Amplifier Circuits, BiCMOS Circuits, Low Power Logic Design, Comparison of Circuit Families, Materials for performance improvement, Techniques for Low power, high speed designs.		

References:

1. Neil Weste and Kamaran, "Principles of CMOS VLSI Design", Education Asia.
2. J. M. Rabaey, A. Chandrakasan and B. Nikolic, Digital Integrated Circuits : A Design Perspective, Pearson (Low Price Edition)
3. Charls Roth, "Digital System Design using VHDL", Tata McGraw Hill.
4. S-M. Kang and Y. Leblebici, CMOS Digital Integrated Circuits : Analysis and Design, Third Edition, McGraw-Hill

Digital CMOS Design

Laboratory Assignments/Experiments:

1. To design, prepare layout and simulate CMOS Inverter for the given specifications of load capacitance, propagation delay, power dissipation, foundry etc.
2. To design logic for ATM machine password and access functionality. Assume suitable I/Os such as card sense, 4 digit PIN number, type of account, amount, other facilities needed etc.
3. To design CMOS logic for F = A + B (C + D) + EFG and prepare layout. Assume suitable capacitive load & foundry. Measure T_R, T_F & $T_{PD.}$
4. To draw FSM diagram, write VHDL code, synthesis, simulate, place & route for Tea/Coffee vending machine. Generalized I/Os of the machine are coin sense, cup sense, option sense, pour valve, timer count, alarm etc. You may assume additional I/Os too.
5. To design and simulate combinational logic to demonstrate hazards. Also, simulate the same logic redesigned for removal of hazards.

Course Outcomes:

1. The student will understand the fundamentals of CMOS Technology in Digital Domain.
2. The student will show the skills of designing digital VLSI.
3. The student will demonstrate the ability for using backend tools in IC technology.

504103	Embedded System Design	
Teaching Scheme: **Lectures 4 Hrs/ Week**		**Examination scheme:** **Theory : 50 Marks (In Semester)** **50 Marks (End Semester)** **Credits : 4**
Module I		
Introduction to Embedded Systems Introduction to Embedded Systems, Architecture of Embedded System, Design Methodology, Design Metrics, General Purpose Processor, System On chip. **Embedded system design and development:** Embedded system design**,** Life-Cycle Models, Problem solving, The design process, Requirement identification, Formulation of requirements specification. Development tools. **System design specifications:** System specifications versus system requirements, Partitioning and decomposing a system, Functional design, Architectural design, Functional model versus architectural model, Prototyping, Other considerations, Archiving the project.		
Module II		
ARM-9 Architecture: ARM-9-TDMI Processor core, ARM architectural support for high level language, ARM architectural support for system development, ARM architectural support for operating System, Memory subsystem architecture, Designing a cache system, Memory allocation, Communication protocols.		
Module III		
Embedded Linux: System architecture, BIOS versus boot-loader, Booting the kernel, Kernel initialization, Space initialization, Boot loaders, Storage considerations **Linux kernel construction**: Kernel build system, Obtaining a custom Linux kernel, File systems, Device drivers, Kernel configuration.		
Module IV		
Android Operating System Introduction to Android technology, Structure of Android applications, Understanding Manifest, Working with Activities, Data stores, Network services and APIs, Intents, Content Providers and services, Advance Operations with Android, Telephony and SMS, Audio Video using the Camera, Project Discussion on Android.		
References:		
1. Steve Furber, "ARM System-on-Chip Architecture", Second Edition, Pearson Education Publication		

2. James K. Peckol, “Embedded Systems: A Contemporary Design Tool”, WILEY Student Edition Publication
3. Tammy Noergaard, “Embedded Systems Architecture”, Elsevier Publication
4. Christopher Hallinan, “Embedded Linux Primer: A Practical Real-World Approach”, Second Edition, Pearson Education Publication
5. Craig Hollabaugh, “Embedded Linux, Hardware, Software and Interfacing”, Pearson Education Publication

Embedded System Design

Laboratory Assignments/Experiments (based on Linux Operating system):

1. Write a program for 4*4 Matrix Keypad Interface.
2. Develop character device driver for GPIO
3. Write a program for on-chip Analog to Digital Conversion.
4. Write a program for I2C based Seven Segment LED Display Interface.
5. Write a program for External Interrupt.

Course Outcomes:

1. The student will study ARM Processor based Embedded System design
2. The student will be able to do programming in Embedded programming in C, C++
3. The student will understand Linux operating system and device driver
4. The student will demonstrate the knowledge of android operating system

504203	Reconfigurable Computing	

Teaching Scheme: Lectures 4Hrs/ Week		Examination scheme: Theory : 50 Marks (In Semester) 50 Marks (End Semester) Credits : 4

Module I

Types of computing and introduction to RC: General Purpose Computing, Domain-Specific Processors, Application Specific Processors; Reconfigurable Computing, Fields of Application; Reconfigurable Device Characteristics, Configurable, Programmable, and Fixed-Function Devices; General-Purpose Computing, General-Purpose Computing Issues;

Module II

Metrics: Density, Diversity, and Capacity; Interconnects, Requirements, Delays in VLSI Structures; Partitioning and Placement, Routing; Computing Elements, LUTs, LUT Mapping, ALU and CLBs; Retiming, Fine-grained & Coarse-grained structures; Multi-context**;**

Module III

Different architectures for fast computing viz. PDSPs, RALU, VLIW, Vector Processors, Memories, CPLDs, FPGAs, Multi-context FPGA, Partial Reconfigurable Devices; Structure and Composition of Reconfigurable Computing Devices: Interconnect, Instructions, Contexts, Context switching, RP space model;

Module IV

Reconfigurable devices for Rapid prototyping, Non-frequently reconfigurable systems, Frequently reconfigurable systems; Compile-time reconfiguration, Run-time reconfiguration; Architectures for Reconfigurable computing: TSFPGA, DPGA, Matrix; Applications of reconfigurable computing: Various hardware implementations of Pattern Matching such as the Sliding Windows Approach, Automaton-Based Text Searching. Video Streaming;

References:

1. Andre Dehon, “Reconfigurable Architectures for General Purpose Computing”.
2. IEEE Journal papers on Reconfigurable Architectures.
3. “High Performance Computing Architectures” (HPCA) Society papers.
4. Christophe Bobda, “Introduction to Reconfigurable Computing”, Springer Publication.
5. Maya Gokhale, Paul Ghaham, “Reconfigurable Computing”, Springer Publication.

Reconfigurable Computing

Laboratory Assignments/Experiments:

1. To Design and implement 2:1 Multiplexer using Transmission Gate.
2. To Design and implement a Full adder using 4:1 Multiplexer.
3. To Design and implement Multi-context (4) 4-LUT and implement using HDL and download on FPGA.
4. To Design and implement 4 bit ALU.
5. To Design and implement the simple Distributed Arithmetic system using HDL.

Course Outcomes:

1. The student will understand concept of static and dynamic reconfiguration.
2. The student will use the basics of the PLDs for designing reconfigurable circuits.
3. The student will understand the reconfigurable system design using HDL

504104	Research Methodology	

Teaching Scheme: Lectures 4Hrs/ Week		Examination scheme: Theory : 50 Marks (In Semester) 50 Marks (End Semester) Credits : 4

Module I

Research Problem

Meaning of research problem, Sources of research problem, Criteria/Characteristics of a good research problem, Errors in selecting a research problem, Scope and objectives of research problem.

Basic instrumentation

Instrumentation schemes, Static and dynamic characteristics of instruments used in experimental set up, Performance under flow or motion conditions, Data collection using a digital computer system, Linear scaling for receiver and fidelity of instrument, Role of DSP is collected data contains noise.

Module II

Applied statistics

Regression analysis, Parameter estimation, Multivariate statistics, Principal component analysis, Moments and response curve methods, State vector machines and uncertainty analysis.

Module III

Modelling and prediction of performance

Setting up a computing model to predict performance of experimental system, Multiscale modelling and verifying performance of process system, Nonlinear analysis of system and asymptotic analysis, Verifying if assumptions hold true for a given apparatus setup, Plotting family of performance curves to study trends and tendencies, Sensitivity theory and applications

Module IV

Developing a Research Proposal

Format of research proposal, Individual research proposal, Institutional proposal. Proposal of a student – a presentation and assessment by a review committee consisting of Guide and external expert only. Other faculty members may attend and give suggestions relevant to topic of research.

References

1. 'Research methodology: an introduction for science & engineering students', by Stuart Melville and Wayne Goddard
2. 'Research Methodology: An Introduction' by Wayne Goddard and Stuart Melville
3. 'Research Methodology: A Step by Step Guide for Beginners', by Ranjit Kumar, 2nd Edition
4. 'Research Methodology: Methods and Trends', by Dr. C. R. Kothari
5. 'Operational Research' by Dr. S.D. Sharma, Kedar Nath Ram Nath & co.

Research Methodology

Laboratory Assignments :

1. Design a typical research problem using scientific method
2. Design a data collection system using digital computer system.
3. Study the various analysis techniques.
4. Design and develop a computing model to predict the performance of experimental system.
5. Develop the following research proposal

   A. Individual B. Institutional

Course Outcomes:

1. The student will learn research problem & its scope, objectives, and errors.
2. The student will learn the basic instrumentation schemes & data collection methods.
3. The student will study the various statistical techniques.
4. The students will study modeling and predict the performance of experimental system.
5. The student will learn to develop the research proposals.

504205	Mathematics for VLSI and Embedded Systems	
ELECTIVE-I		
Teaching Scheme: **Lectures 4Hrs/ Week**		**Examination Scheme:** **Theory : 50 Marks (In Semester)** **50 Marks (End Semester)** **Credits : 4**

Module I

Mathematical Modelling Through Graphs, Mathematical modelling: Need, techniques, Classification and simple illustrations, Fundamental concepts of graph, optimization and trees, optimization and complexity, Advanced matrix theory

Module II

Eigen-values using QR transformations – Generalized Eigen vectors – Canonical forms – Singular value decomposition and applications – Pseudo inverse – Least square approximations. Linear programming, Formulation – Graphical Solution – Simplex Method – Two Phase Method

Module III

Probability, relative frequency, Joint and conditional probability, Baye's theorem, Independent events, permutations and combinations, Random variables, Probability density function, histogram, Cumulative distribution function, Standard probability density functions

Module IV

Gaussian variable, uniform exponential and Rayleigh distribution, Binomial and Poisson distribution, fitting a distribution function to a random variable, Chi square test, K_S test, Operations on random variables, expected value, Moments, centre moments, skew and Kurtosis, characteristic function, moment generating function, computer generation of a random variable, central limit theorem

References

1. Mathematical Modeling J N Kapur New Age International Publisher
2. Introduction to Graph Theory second Edition by Douglas B. West, Pearson Education Asia.
3. Bronson, R., Matrix Operation, Schaum's outline series, McGraw Hill, New York, (1989).
4. Taha, H. A., Operations Research: An Introduction, Seventh Edition, Pearson Education Edition, Asia, New Delhi (2002).
5. Peyton Peebles, Probability, random variables and random signal principles, 4th edition, TMH publications

Mathematics for VLSI and Embedded Systems

Laboratory Assignments/Experiments:

1. Demonstrate the feature extraction of a typical image using singular value decomposition technique.
2. Describe a typical case study using Bay's theorem.
3. Describe probability density function using suitable example.
4. Describe Binomial and Poisson distribution using suitable example.
5. Explain central limit theorem.

Course Outcomes:

1. The student will be capable of Mathematical modeling through graph.
2. The student will study fundamental to solutions and related methods.
3. The student will exhibit the knowledge of Probability based mathematical aspects.
4. The student will study various distributions.

504205	Neural Networks in Embedded Applications	
ELECTIVE-I		
Teaching Scheme: **Lectures 4Hrs/ Week**		**Examination Scheme:** **Theory : 50 Marks (In Semester)** **50 Marks (End Semester)** **Credits : 4**

Module I

Introduction to artificial neural networks, Fundamental models of artificial neural network, Perceptron networks, Feed forward networks, Feedback networks, Radial basis function networks, Associative memory networks

Module II

Self organizing feature map, Learning Vector Quantization, Adaptive resonance theory, Probabilistic neural networks, neocgnitron, Boltzmann Machine

Module III

Optical neural networks, Simulated annealing, Support vector machines, Applications of neural network in Image processing, Introduction to Embedded systems, Characteristic

Module IV

Features and Applications of an embedded system, Introduction to embedded digital signal processor, Embedded system design and development cycle, ANN application in digital camera, Implementation of Radial Basis Function, Neural Network on embedded system: real time face tracking and identity verification, Overview of design of ANN based sensing logic and implementation for fully automatic washing machine

References

1. S N Sivanandam, S Sumathi, S N Deepa, "Introduction to Neural Networks Using Matlab 6.0", Tata McGraw Hill Publication
2. Simon Haykin, "Neural Networks: Comprehensive foundation", Prentice Hall Publication
3. Frank Vahid, TonyGivargis, "Embedded System Design A unified Hardware/ Software Introduction", Wiley India Pvt. Ltd.
4. Rajkamal, "Embedded Systems Architecture, Programming and Design," Tata McGraw-Hill

Neural Networks in Embedded Applications

Laboratory Assignments/Experiments:

1. Generation of AND, OR, NOT and OR gate using MP model.
2. Implementation of AND gate using single layer perception.
3. Implementation of various learning rules.
4. Verification of back propagation algorithm.
5. Implementation of RBF neural network in embedded system.

Course Outcomes:

1. The student will use analogy of human neural network for understanding of artificial learning algorithms.
2. The student will study fundamental models.
3. The student will exhibit the knowledge of radial basis function network.

504205	Processor Design	
ELECTIVE-I		
Teaching Scheme: **Lectures 4Hrs/ Week**		**Examination Scheme:** **Theory : 50 Marks (In Semester)** **50 Marks (End Semester)** **Credits : 4**

Module I

Embedded Computer Architecture Fundamentals: Components of an embedded computer, Architecture organization, ways of parallelism, I/O operations and peripherals. Problems, Fallacies, and Pitfalls in Processor Design for a high level computer instruction set architecture to support a specific language or language domain, use of intermediate ISAs to allow a simple machine to emulate it's betters, stack machines ,overly aggressive pipelining ,unbalanced processor design, Omitting pipeline interlocks, Non-power-of-2 data-word widths for general-purpose computing

Module II

Memory: Organization, Memory segmentation, Multithreading, Symmetric multiprocessing.

Processor Design flow: Capturing requirements, Instruction coding, Exploration of architecture organizations, hardware and software development. Extreme CISC and extreme RISC ,Very long instruction word (VLIW),

Module III

Digital signal processor: Digital signal processor and its design issues, evolving architecture of DSP, next generation DSP.

Customizable processors: Customizable processors and processor customization, A benefit analysis of processor customization, use of microprocessor cores in SOC design, benefits of microprocessor extensibility.

Module IV

Run time Re-configurable Processors : Run time Re-configurable Processors ,Embedded microprocessor trends, instruction set metamorphosis, reconfigurable computing, run-time reconfigurable instruction set processors ,coarse grain reconfigurable processors,

Processor Clock Generation and Distribution: Clock parameters and trends, Clock distribution networks, de-skew circuits, jitter reduction techniques, low power clock distribution

Asynchronous Processor Design: Asynchronous and self timed processor design, need of asynchronous design, development of asynchronous processors, asynchronous design styles, features of asynchronous design.

References

1. Jari Nurmi, Processor Design-System on Chip Computing for ASIC's and FPGA, Springer Publications.
2. G. Frantz, The DSP and It's Impact on the Technology.
3. S. Leibson,Tensilica, Customizable Processors and Processor Customization ,
4. F. Campi , Run-Time Reconfigurable Processors

5. J. Garside, S. Furber , Asynchronous and Self-Timed Processor Design.
6. S. Rusu, Processor Clock Generation and Distribution.
7. Andre Dehon, Reconfigurable Architecture for General purpose Computing.

Processor Design

Laboratory Assignments/Experiments:

1. Design and implement MAC Unit on PLD
2. Design and implement CPU on PLD
3. Design and implement Carry look-ahead generator on PLD
4. Design and implementation of Translation look-aside buffer.

Course Outcomes:

1. The student will learn Problems, Fallacies and Pitfalls in Processor Design.
2. The student will study Extreme CISC and extreme RISC, Very Long Instruction Word (VLIW), overly aggressive pipelining, unbalanced processor.
3. The student will show skills to implement Processor functional components like MAC.

504205	Wireless Sensor Network	
ELECTIVE-I		
Teaching Scheme: **Lectures 4 Hrs/ Week**		**Examination Scheme:** **Theory : 50 Marks (In Semester)** **50 Marks (End Semester)** **Credits : 4**

Module I

Introduction : Motivation for a Network of Wireless Sensor Nodes , Sensing and Sensors Wireless Networks, Challenges and Constraints

Applications : Health care, Agriculture, Traffic and others

Module II

Architectures : Node Architecture; the sensing subsystem, processor subsystem, communication interface, LMote, XYZ, Hogthrob node architectures

Power Management - Through local power, processor, communication subsystems and other means, time Synchronization need, challenges and solutions overview for ranging techniques.

Security Fundamentals, challenges and attacks of Network Security, protocol mechanisms for security.

Module III

Operating Systems -Functional and non functional Aspects, short overview of prototypes – Tiny OS, SOS, Contiki, LiteOS, sensor grid.

Module IV

Physical Layer- Basic Components, Source Encoding, Channel Encoding, Modulation, Signal Propagation

Medium Access Control – types, protocols, standards and characteristics, challenges

Network Layer -Routing Metrics, different routing techniques

References

1. Dargie, W. and Poellabauer, C., "Fundamentals of wireless sensor networks: theory and practice", John Wiley and Sons, 2010
2. Sohraby, K., Minoli, D., Znati, T. "Wireless sensor networks: technology, protocols, and applications, John Wiley and Sons", 2007
3. Hart, J. K. and Martinez, K. (2006) Environmental Sensor Networks: A revolution in the earth system science? Earth-Science Reviews, 78.
4. Protocols and Architectures for Wireless Sensor Networks Holger Karl, Andreas Willig - 08-Oct-2007

5. Wireless Sensor Networks: An Information Processing Approach Feng Zhao, Leonidas J. Guibas - 06-Jul-2004 - 358 pages

Wireless Sensor Network

Laboratory Assignments/Experiments:

1. Reading data from sensor node.
2. Implement 50 stationary nodes topology using NS2 for data transmission and record QOS parameters of the networks/ test bed.
3. Implement 50 dynamic nodes topology using NS2 for data transmission and record QOS parameters of the networks / test bed.
4. On any above topology change the network layer/transport layer/MAC layer protocol and monitor the changes between any two protocols/ test bed using Network Simulator.

Course Outcomes:

1. The student will understand the architecture of WSN network.
2. The student will understand the physical layer related aspects of WSN network.
3. The student will exhibit the knowledge of power management in wireless communication systems.
4. The student will exhibit the knowledge of security aspects of WSN systems.

504205	***LATEX**	
ELECTIVE-I		
Teaching Scheme: Theory 1 Hrs/ Week		**Examination Scheme: Credits :1**

LaTeX /Document Structure, Document classes, Packages, The document environment, Book structure.

References:

http://miktex.org/
http://www.winedt.com/

*For each Subject under Elective I the student Shall study LATEX for 1 credit.

504206	Lab Practice I	
Teaching Scheme: **Practical 4 Hrs/ Week**		**Examination Scheme:** **Term Work : 50 Marks** **Oral/ Presentation: 50 Marks** **Credits :4**
Lab Practice I: The laboratory work will be based on completion of minimum two assignments/experiments confined to the courses of that semester.		

SEMESTER-II

504207	Analog CMOS Design	
Teaching Scheme: Lectures 4 Hrs/ Week		**Examination scheme: Theory : 50 Marks (In Semester) 50 Marks (End Semester) Credits : 4**
Module I		
Current sources and References MOSFET as switch, diode and active resistor; MOS Small-signal Models, Common Source Amplifier, The CMOS Inverter as an Amplifier, Weak inversion; Short channel regime; Current sinks and sources; Current mirrors; Current and voltage references, band gap reference.		
Module II		
CMOS Opamp Inverters, cascode and differential amplifiers; Output amplifier; Opamp, high speed opamp, micro power opamp, low noise opamp.		
Module III		
Low and High Bandwidth Design Digital to Analog Converters, switched capacitors, Analog to Digital Converters, Bandwidth estimation open and short circuit techniques; Zeros as bandwidth enhancers; Tuned amplifiers.		
Module IV		
Low Noise Amplifier Low Noise Amplifier (LNA) design, noise and power trade off, optimizations; Design of mixer; Advanced trends in Radio Frequency (RF) chip design.		
References		

1. Thomas Lee, "The Design of CMOS Radio – Frequency Integrated Circuits", Second edition, Cambridge.
2. B. Razavi, *Design of Analog CMOS Integrated Circuits*, McGraw-Hill
3. P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*, Second Edition, Oxford University Press
4. P. Gray, P. J. Hurst, S. H. Lewis and R. Meyer, *Analysis and Design of Analog Integrated Circuits*, Fourth Edition,Wiley, 2001. (Low Price Edition)

Analog CMOS Design

Laboratory Assignments/Experiments:

1. To design cascode current mirror for output current of 100 µA. Prepare layout and simulate. Comment on output resistance.
2. To design, prepare layout and simulate CMOS differential amplifier for CMRR of 40 dB. Comment on ICMR.
3. To design, prepare layout and simulate multistage CMOS RF amplifier in 90 nm technology for voltage gain of 60 dB, bandwidth of 100 MHz, and source impedance of 50 Ω.
4. To design CMOS RF amplifier for voltage gain of 60 dB. Suggest and design suitable technique to enhance the bandwidth. Simulate each added technique step by step. Comment on the improvement resulted each time. Prepare layout of the final schematic and simulate.
5. List the sources of cross talk. Explore in detail, the existence of cross talk in each case. What are the mitigation techniques? Prepare case study for one of them. Verify the cross talk and its mitigation through simulation.

Course Outcomes:

1. The student will understand the fundamentals of CMOS Technology in Analog Domain.
2. The student will show the skills of designing CMOS analog circuits.
3. The student will demonstrate the ability for using backend tools in analog IC technology.

504208	System on Chip	

Teaching Scheme: Lectures 4 Hrs/ Week		Examination scheme: Theory : 50 Marks (In Semester) 50 Marks (End Semester) Credits : 4

Module I

Basic Concepts: The nature of hardware and software, data flow modelling and implementation, the need for concurrent models, analyzing synchronous data flow graphs, control flow modelling and the limitations of data flow models, software and hardware implementation of data flow, analysis of control flow and data flow, Finite State Machine with data-path, cycle based bit parallel hardware, hardware model , FSMD data-path , simulation and RTL synthesis, language mapping for FSMD.

Module II

Micro-programmed Architectures : limitations of FSM , Micro-programmed : control, encoding , data-path, Micro-programmed machine implementation , handling Micro-program interrupt and pipelining , General purpose embedded cores , processors, The RISC pipeline, program organization, analyzing the quality of compiled code, System on Chip, concept, design principles , portable multimedia system, SOC modelling, hardware/software interfaces , synchronization schemes, memory mapped Interfaces , coprocessor interfaces, coprocessor control shell design, data and control design, Programmer's model .

Module III

RTL intent : Simulation race, simulation-synthesis mismatch, timing analysis, timing parameters for digital logic, factors affecting delay and slew, sequential arcs, clock domain crossing ,bus synchronization , preventing data loss through FIFO, Importance of low power, causes and factors affecting power, switching activity, simulation limitation, implication on synthesis and on backend.

Module IV

Research topics in SOC design: A SOC controller for digital still camera, multimedia IP development image and video CODECS, soc memory system design, embedded software, and energy management techniques for SOC design, SOC prototyping, verification, testing and physical design.

References

1. Patrick R. Schaumont, "A Practical Introduction to Hardware/Software Co design", Springer
2. Sanjay Churiwala, Sapan Garg , "Principles of VLSI RTL Design A Practical Guide", Springer
3. Youn-Long Steve Lin, "Essential Issues in SOC Design, Designing Complex Systems-on-Chip", Springer

4. Wayne Wolf, "Modern VLSI Design Systems on Chip", Pearson Education
5. Rajanish K. Kamat, Santhosh A. Shinde, Vinod G. Shelake, "Unleash the System On Chip using FPGAs and Handel C", Springer

System on Chip

Laboratory Assignments/Experiments:

1. Design, simulate and implement FSM on PLD for detection of either of input sequence X = … 1001... . or …1101… sequence and set output flags Y = '1' or Z='1' respectively. What is effect on area, speed, fan out and power by implementing this design using different state encoding styles?
2. Design and implement MOD4 counter on PLD and verify multi-clock operations by probing logic analyzer.

Control bits	Count update after every sec.
00	0.25 sec
01	0.5 sec
10	1 sec
11	4 sec

3. Why gated clock is not preferred in digital design? Write Verilog code to implement CMOS layout which will generate glitch also design a RTL by Write VHDL will generate glitch and also measure it using electronic test equipment.
4. Implement temperature logging system as a co-design by Interfacing FPGA & μC 8051 as follows :
   i) LM 35 interfaced with ADC
   ii) ADC interfaced with FPGA
   iii) FPGA interfaced with μC 8051
   iv) μC 8051 is interfaced with LCD

To display real-time room temperature. If temperature is greater than 25^0 C Bi-colours LED should change its normal Green color to RED color via opto-isolator by actuation of relay.

Course Outcomes:

1. The student will learn to design flow graphs and flow modeling.
2. The student will study SOC modeling and interfacing.
3. The student will learn SOC memory system design, embedded software and energy management techniques for SOC design, SOC prototyping, verification, testing and physical design.
4. The student will able to design , implement and test SOC.

504209	Embedded Signal Processors	

Teaching Scheme: Lectures 4 Hrs/ Week		Examination scheme: Theory : 50 Marks (In Semester) 50 Marks (End Semester) Credits : 4

Module I

Introduction to Real-Time Embedded Signal Processing, Time-Domain Digital Signals, Introduction to Digital Systems, Moving-Average Filters: Structures and Equations, Digital Filters Realization of FIR Filters, Nonlinear Filters Implementation.

Module II

Frequency-Domain Analysis and Processing, Discrete Fourier Transform, Fast Fourier Transform, Simple Low pass Filters Design and applications of Notch Filters, Design of FIR Filters Design of IIR Filters, Structures and Characteristics of IIR Filters, Algorithms of Adaptive Filters, Design and Applications of Adaptive Filters.

Module III

Introduction to Digital signal processing systems, MAC, Barrel shifter, ALU, Multipliers, Dividers, DSP processor architecture, Software developments, Selections of DSP processors, Hardware interfacing, DSP processor architectures: TMS 320C54XX, TMS 320C67XX Blackfin processor: Architecture overview, memory management, I/O management, On chip resources, programming considerations, Real time implementation Considerations, Memory System and Data Transfer, Code Optimization

Module IV

Practical DSP Applications: Audio Coding and Audio Effects, Digital Image Processing, Two-Dimensional Filtering, Image Enhancement, DTMF generation and detection, FFT algorithms, Wavelet algorithms, Adaptive algorithms: system identification, inverse modeling, noise cancellation, prediction..

References

1. Woon-Seng Gan and Sen M. Kuo, "Embedded Signal Processing With the Micro Signal Architecture", Wiley-IEEE Press 2007
2. Sen M. Kuo and Woon-Seng Gan, " Digital Signal Procesors: architectures, implementations and applications", Prentice-Hall.
3. Sanjit K. Mitra, " Digital Signal Processing: A Computer based approach", McCraw Hill, 1998.
4. Lawrence R. Rabiner and Bernard Gold, "Theory and application of Digital signal Processing", Prentice-Hall of India, 2006.

Embedded Signal Processors

Laboratory Assignments/Experiments:

1. Design and simulate N point FFT by targeting suitable DSP processor platform.
2. Design and simulate N tap FIR filter by targeting suitable DSP processor platform.
3. Design and simulate LMS adaptive filter.
4. Performance comparison of different filter structures.

Course Outcomes:

1. The student will be capable of designing the system for linear filtering using DFT.
2. The student will show skills for design of FIR and IIR filters for any application.
3. The student will exhibit the knowledge of implementing DSP algorithms on DSP Processor Platforms.
4. The student will demonstrate the design of adaptive filters.
5. The student will demonstrate the ability to analyze filter structures.

504210	Embedded Product Design	
ELECTIVE-II		
Teaching Scheme: **Lectures 4 Hrs/ Week**		**Examination Scheme:** **Theory : 50 Marks (In Semester)** **50 Marks (End Semester)** **Credits : 4**

Module I

Overview of embedded products: Need, Design challenges, product survey, specifications of product need of hardware and software, Partitioning of the design into its software and hardware components, Iteration and refinement of the partitioning.

Module II

Deign models and techniques: various models of development of hardware and software, their features, different Processor technology, IC technology, Design Technology.

Module III

Modules of H/W.S/W: Tradeoffs, Custom Single-purpose processors, General-purpose processors, Software, Memory, Interfacing, Design technology-Hardware design, FPGA design, firmware design, driver development, RTOS porting, cost reduction, re-engineering, optimization, maintenance, validation and development, prototyping, turnkey product design.

Module IV

Testing and verification: Embedded products-areas of technology, Design and verification, Integration of the hardware and software components, testing- different tools, their selection criterion

Certification and documentation: Mechanical Packaging, Testing, reliability and failure analysis, communication protocols, Certification (EMI / RFI) and Documentation. Study of any TWO real life embedded products in detail.

References

1. Frank Vahid and Tony Givargis , "Embedded System Design: A Unified Hardware/Software Introduction", John Wiley publication
2. P Marwedel, "Embedded System Design", Springer publication

Embedded Product Design

Laboratory Assignments/Experiments:

1. To estimate techno-commercial feasibility of any one embedded product such as mobile phone, programmable calculator, tablet PC, biometrics system, set top box etc.
2. To study design considerations of any one embedded product e.g. laptop, video conferencing system, surveillance/ security system, EMG/ECG machine etc.
3. To design any one embedded product to solve any real life problem/s.
4. To test the hardware designed for above assignment (3) using suitable tool.
5. To simulate the software designed for the above assignment (3) using suitable tool.

Course Outcomes:

1. The student will study Embedded System & Product specifications, challenges
2. The student will be able to do cost estimation of Embedded product
3. The student will understand the aspects of Mechanical Packaging, Testing, reliability and failure analysis, Certification (EMI / RFI) and Documentation
4. The student will demonstrate the knowledge embedded product design related hardware and software design tools.

504210	VLSI Interconnections	
ELECTIVE-II		
Teaching Scheme: Lectures 4 Hrs/ Week		**Examination Scheme: Theory : 50 Marks (In Semester) 50 Marks (End Semester) Credits : 4**

Module I

Metal interconnects, Transmission line equations, Analysis of tree structure, Interconnect model based on scattering matrix.

Module II

Propagation modes, slow wave mode; Parasitic inductances, capacitances, resistances, Ground planes.

Module III

Propagation modes, slow wave mode; Parasitic inductances, capacitances, resistances, Ground planes, Green's function method; Interconnect delays

Module IV

Micro strip line model, Analysis, RC models, RLC models; Electromagnetic analysis of multi conductor interconnects; Mesh interconnects, hierarchical interconnects. Switch box routing in PLDs, Optimizations; Future interconnects, Optical interconnects, super conducting interconnects, Nano technology circuit interconnects.

References

1. Ashok K. Goyal, "High Speed VLSI Interconnections", Second Edition, IEEE Press, John Wiley Publications
2. Michel S. Nakhla, O. J. Zhang, "Modeling and Simulation of High Speed VLSI Interconnects", Springer Publication

VLSI Interconnections

Laboratory Assignments/Experiments:

1. Simulate RC circuit and comment on transient response.
2. Simulate startup model of RLC.
3. Simulate a transmission line and evaluate VSWR, Reflection coefficient parameters considering different loading considerations using analog simulation tool.
4. Plot stability circle, for given values of S parameters.

Course Outcomes:

1. The student will understand the interconnect models.
2. The student will study delay aspects due to high speed operations.
3. The student will study futuristic aspects of interconnection.

504210	Mixed Signal Circuit Design	
ELECTIVE-II		
Teaching Scheme: **Lectures 4 Hrs/ Week**		**Examination Scheme:** **Theory : 50 Marks (In Semester)** **50 Marks (End Semester)** **Credits : 4**

Module I

Analog versus discrete time signals, Converting analog signal to digital signal, Sample and hold characteristics, DAC specifications, ADC specifications, Mixed signal layout issues: floor planning, power supply and grounding issues, fully differential design/ matching, guard rings, shielding, interconnect considerations**.**

Module II

DAC architectures: Resistor string, R-2R ladder networks, Current steering, Charge-scaling, Pipeline. ADC architectures: Flash, Pipeline, Dual slope, Successive approximation, Oversampling ADC.

Module III

Data converter modelling: Sampling and aliasing: A modelling approach, Impulse sampling, AAF and RCF, Time domain description of reconstruction, The sample and hold, S/H spectral response, Circuit concerns for implementing S/H. Quantization noise, RMS quantization noise voltage, treating quantization noise as a random variable, calculating RMS quantization noise voltage from a spectrum

Module IV

Data converter SNR: Effective number of bits, Signal to noise plus distortion ratio, Spurious free dynamic range, dynamic range, SNR & SNDR, Clock jitter, Averaging to improve SNR, Spectral density view, Jitter and averaging, Relaxed requirements on AAF, Data converter linearity requirements, Adding noise dither to ADC input, Decimating filters for ADC. Decimating filters for ADCs, Interpolating filters for DACs. Noise-shaping data converters: First order noise shaping, Second order noise shaping, Noise shaping topologies: Higher-order modulators, Miltibit modulators, Cascaded modulators.

References

1. R. Jacob Baker, “CMOS: Mixed Signal Circuit Design”, 2nd edition, Wiley IEEE press publications.
2. R. Jacob Baker, “CMOS: Circuit Design, layout and simulation”, 2nd edition, Wiley IEEE press publications.
3. Allen, Phillip E., Holberg, Douglus R., “CMOS Analog Circuit Design”, Oxford University Press publications.

Mixed Signal Circuit Design

Laboratory Assignments/Experiments:[Perform any 5]

1. Plot ideal transfer curves for 3 bit and 4 bit DAC, using V_{Ref} = 5V and 3V. Find the resolution for a DAC if the output voltage is desired to change in 1 mV increments.
2. For 3 bit ADC, V_{Ref} = 5V, Plot ideal transfer curve and quantization error.
3. Plot transfer curve and quantization error by shifting entire transfer curve of example 2, left by 1/2 LSB and calculate DNL.
4. Design and simulate anti-aliasing filter with two input sine waves having frequencies 4MHz & 40 MHz.
5. Design and simulate sample and hold circuit, with 8 MHz sine wave sampled at 100 MHz.
6. Calculate SNR and plot ADC input and DAC output for cascaded 8 bit ADC and DAC operated on VDD=1.5 V, Vin = 24 MHZ (0.75VPP), Sampling frequency = 100 MHz.

Course Outcomes:

1. The student will understand the issues mixed signal issues in circuit design.
2. The student will understand types and modeling of ADCs & DACs.
3. The student will understand methods to improve SNR.
4. The student will understand delta-sigma or sigma-delta converter, and its issues.

504210	Software Defined Radio	
ELECTIVE- II		
Teaching Scheme: **Lectures 4 Hrs/ Week**		**Examination Scheme:** **Theory : 50 Marks (In Semester)** **50 Marks (End Semester)** **Credits : 4**

Module I

Fundamentals of SDR: Software Radios, Needs, Characteristics, Benefits, Design Principles of a Software Radio, Radio frequency implementation issues, Principal Challenge of Receiver Design

Module II

RF and SDR: RF Receiver Front-End Topologies, Enhanced Flexibility of the RF Chain with Software Radios, Transmitter Architectures and their issues, Noise and Distortion in the RF Chain, Timing Recovery in Digital Receivers Using Multirate Digital Filters

Module III

Signals in SDR: Approaches to Direct Digital Synthesis, Analysis of Spurious Signals, Spurious Components due to Periodic Jitter, Band-pass Signal Generation, Hybrid DDS-PLL Systems, Generation of Random Sequences, Parameters of data converters

Module IV

Smart Antennas: Concept of Smart Antennas, Structures for Beam-forming Systems, Smart Antenna Algorithms, Digital hardware choices, Key Hardware Elements, DSP Processors, Field Programmable Gate Arrays, Trade-Offs in Using DSPs, FPGAs and ASICs

Case studies in Radio System: Power Management Issues, Object-oriented representation of radios and network resources, Mobile Application Environments, Joint Tactical Radio System, Case studies in software radio design.

References

1. Jeffrey H. Reed, "Software Radio: A Modern Approach to Radio Engineering", Prentice Hall PTR; May 2002 ISBN: 0130811580
2. Dillinger, Madani, Alonistioti (Eds.), "Software Defined Radio, Architectures, Systems and Functions", Wiley 2003
3. Bard, Kovarik, "Software Defined Radio, The Software Communications Architecture", Wiley 2007
4. Johnson, C.R. and W.A. Sethares, "Telecommunication Breakdown: Concepts of Communication Transmitted via Software-Defined Radio, Pearson Prentice Hall, 2004
5. Bard, John and Kovarik, Vincent, "Software Defined Radio: The Software Communications Architecture", Wiley Series in Software Radio, 2007

Software Defined Radio

Laboratory Assignments/Experiments:

1. Design and simulate OFDM system for given specifications.
2. Design and simulate PSK module for given specifications; calculate performance measures.
3. Design and simulate PLL system for given specifications.
4. Design and simulate high resolution ADC, find DNL, INL, & SNR for given specifications.

Course Outcomes:

1. The student will study Needs, Characteristics, Benefits and Design Principles of a Software Radio.
2. The student will be study design aspects of software radios.
3. The student will understand concept of Smart Antennas.
4. The student will study key hardware elements and related Trade-Offs.

504210	***Software Tools**	
ELECTIVE-II		
Teaching Scheme: **Theory 1 Hrs/ Week**		**Examination Scheme:** **Credits :1**
Introduction to software tools such as Octave, MATLAB, LAB VIEW, RTLinux, VxWorks, µCOS-II, Tiny OS, ANDROID, Xilinx, Microwind, Tanner, TCAD Tools, NS-II, NS-III, OMNET++, OPNET, AWR Microwave office, CAD Feko, IE-3D.		
*For each Subject under Elective II the student Shall study open source/evaluation versions of at least two software tools mentioned above and should present term paper.		

504211	Lab Practice II	
Teaching Scheme: **Practical 4 Hrs/ Week**		**Examination Scheme:** **Term Work : 50 Marks** **Oral/ Presentation: 50 Marks** **Credits :4**
Lab Practice II: The laboratory work will be based on completion of minimum two assignments/experiments confined to the courses of the semester.		

504212	Seminar I	
Teaching Scheme: **Practical 4 Hrs/ Week**		**Examination Scheme:** **Term Work : 50 Marks** **Oral/ Presentation: 50 Marks** **Credits :4**
Seminar I : Shall be on state of the art topic of student's own choice approved by an authority. The student shall submit the duly certified seminar report in standard format, for satisfactory completion of the work by the concerned Guide and head of the department/institute.		

SEMESTER-III

604201	Fault Tolerant Systems	
Teaching Scheme: **Lectures :04/week**		**Examination scheme:** **Theory : 50 Marks (In Semester)** **50 Marks (End Semester)** **Credits : 4**

Module I

Modelling and Logic Simulation:
Functional modelling at the logic and the register level, Structural models, Level of modelling. Type of simulation, unknown logic value, compiled simulation, Event-driven simulation, different delay models, Hazard Detection.

Module II

Fault Modelling and Fault Simulation:
Logical fault models, Fault detection and Redundancy, Fault equivalence and fault location, Fault Dominance, Single stuck-fault models, Multiple stuck fault model, stuck RTL variables, Fault variables. Testing for single stuck fault and Bridging fault, General fault simulation techniques, Serial and Parallel fault simulation, Deductive fault simulation, Concurrent fault simulation, Fault simulation for combinational circuits, Fault sampling, Statistical fault analysis.

Module III

Compression techniques and Self checking System:
General aspects of compression techniques, ones- count compression, transition – count compression, Parity – check compression, Syndrome testing and Signature Analysis, Self checking Design, Multiple – Bit Errors, self– checking checkers, Parity – check function , totally self-checking m/n code checkers, totally self-checking equality checkers, Self-checking Berger code checkers and self checking combinational circuits.

Module IV

Testability:
Testability, trade- offs, Ad hoc Design for Testability techniques, Introduction to BIST concept, Test pattern generation for BIST, Self testing circuits for systems, memory & processor testing, PLA-testing, automatic test pattern generation and Boundary Scan Testing JTAG.

References

1. M.Abramovici, M.A. Breuer, A.D. Friedman, “Digital systems testing and testable design”, Jaico Publishing House.
2. Kwang-Ting (Tim) Cheng and Vishwani D. Agrawal, “Unified Methods for VLSI Simulation and Test Generation” The Springer International Series in Engineering (Jun 30, 1989).

Fault Tolerant Systems

Laboratory Assignments/Experiments:

1. Simulate a single input signature analyzer for given characteristic equation and input sequence.
2. Implement different compression techniques like ones- count, transition- count.
3. Implement self checking system in automatic detection of fault.
4. Implement different fault models using back end tool.
5. Design event driven simulation model using VLSI simulation software.

Course Outcomes:

1. The student will learn functional modeling.
2. The student will use theory of logical fault models for testing single stuck fault.
3. The student will show skills for fault simulation for statistical fault analysis.
4. The student will exhibit the knowledge of self-checking for design of self-checking combinational circuits.
5. The student will exhibit the self-testing for memory, processor and PLA.

604202	ASIC Design	
Teaching Scheme: **Lectures 04/week**		**Examination scheme:** **Theory : 50 Marks (In Semester)** **50 Marks (End Semester)** **Credits : 4**

Module I

Introduction to ASIC :
Introduction to ASIC, Types of ASIC, ASIC Design flow, Comparison between ASIC technologies,ASIC cell libraries. Design entry by VHDL, Modelling of combinational and sequential circuits, Logic synthesis and logic simulations like static timing analysis, functional simulation and Test benches.

Module II

Mixed Signal ASIC Design **:**
Mixed Signal ASIC Design, practical aspects of mix analog digital design, gate level mixed mode simulation, synthesis and testing. A brief introduction to signal integrity effects in ASIC design.

Module III

ASIC construction **:**
ASIC construction with goals, objectives and various algorithms for system partitioning, floor-planning, placement and routing, Parameter extraction with Post layout simulation and Pre layout simulation.

Module IV

Testing techniques used in ASIC **:**
Testing techniques used in ASIC like Automatic test pattern generation, Scan test, Built in self test and JTAG. Brief view of Stuck at fault models and fault simulation. ASIC Verification and its issues, Types and features of existing available EDA tool.

References

1. Michael Smith, "Application Specific Integrated Circuits" Pearson Education Asia
2. R.S. Soin, F. Maloberti and J. Franca, "Analogue-digital ASICs: circuit techniques, design tools and applications", IEE Publications
3. Raminderpal Singh, "Signal Integrity Effects in Custom IC and ASIC Designs", Wiley Publications

ASIC Design

Laboratory Assignments/Experiments:

1. Write VHDL code to simulate, synthesis, place & route priority encoder on PLD. Check the results and also write the test bench.
2. Write VHDL code to simulate, synthesis, place & route RAM/FIFO on PLD. Check the results and also write the test bench.
3. Draw CMOS layout & simulate Full adder/ MUX by applying DRC's of appropriate foundry using backend tool and check the outputs.
4. Draw CMOS layout & simulate 3 bit counter / Shift register by applying DRC's of appropriate foundry using backend tool and check the outputs.
5. Simulate stuck-at fault model of a given function.

Course Outcomes:

1. The student will understand the skills of designing analog and digital ASICs.
2. The student will use the basics of the PLDs for designing IP Cores.
3. The student will understand the ASIC testing.

604204	Seminar II	
Teaching Scheme: **Practical 4 Hrs/ Week**		**Examination Scheme:** **Term Work : 50 Marks** **Oral/ Presentation: 50 Marks** **Credits :4**
Seminar II : shall be on the topic relevant to latest trends in the field of concerned branch, preferably on the topic of specialization based on the electives selected by him/her approved by authority. The student shall submit the seminar report in standard format, duly certified for satisfactory completion of the work by the concerned guide and head of the Department/Institute.		

604205	Project Stage- I	
Teaching Scheme: **Practical 8 Hrs/ Week**		**Examination Scheme:** **Term Work : 50 Marks** **Oral/ Presentation: 50 Marks** **Credits :8**
Project Stage – I Project Stage – I is an integral part of the project work. In this, the student shall complete the partial work of the project which will consist of problem statement, literature review, project overview, scheme of implementation (Mathematical Model/SRS/UML/ERD/block diagram/ PERT chart, etc.) and Layout & Design of the Set-up. As a part of the progress report of Project work Stage-I, the candidate shall deliver a presentation on the advancement in Technology pertaining to the selected dissertation topic. The student shall submit the duly certified progress report of Project work Stage-I in standard format for satisfactory completion of the work by the concerned guide and head of the Department/Institute.		

ELECTIVE-III

Select one subjects from Group-I, and one subject from Group-II from the following list as Elective-III.

Group		Subject	Credit
I	1	Value Education, Human Rights and Legislative Procedures	3
	2	Environmental Studies	3
	3	Energy Studies	3
	4	Disaster Management	3
	5	Knowledge Management	3
	6	Foreign Language	3
	7	Economics for Engineers	3
	8	Engineering Risk – Benefit Analysis	3
II	1	Technology Play	2
	2	Optimization Techniques	2
	3	Fuzzy Mathematics	2
	4	Design and Analysis of Algorithms	2
	5	CUDA	2

604103	Value Education, Human Rights and Legislative Procedures	Group I
ELECTIVE- III		
Teaching Scheme: **Lectures 3 Hrs/ Week**		**Examination Scheme:** **Theory :** **50 Marks (In Semester)** **50 Marks (End Semester)** **Credits : 3**

Module I

Values and Self Development-Social values and individual attitudes, Work ethics, Indian vision of humanism, Moral and non moral valuation, Standards and principles, Value judgments. Importance of cultivation of values, Sense of duty, Devotion, Self reliance, Confidence, Concentration, Truthfulness, Cleanliness, Honesty, Humanity, Power of faith, National unity, Patriotism, Love for nature, Discipline.

Module II

Personality and Behavior Development- Soul and scientific attitude, God and scientific attitude, Positive thinking, Integrity and discipline, Punctuality, Love and kindness, Avoiding fault finding, Free from anger, Dignity of labor, Universal brotherhood and religious tolerance, True friendship, Happiness vs. suffering love for truth, Aware of self destructive habits, Association and cooperation, Doing best, Saving nature.

Module III

Human Rights- Jurisprudence of human rights nature and definition, Universal protection of human rights, Regional protection of human rights, National level protection of human rights, Human rights and vulnerable groups.

Legislative Procedures- Indian constitution, Philosophy, fundamental rights and duties, Legislature, Executive and Judiciary, Constitution and function of parliament, Composition of council of states and house of people, Speaker, Passing of bills, Vigilance, Lokpal and functionaries

References:

1. Chakraborty, S.K., Values and Ethics for Organizations Theory and Practice, Oxford University Press, New Delhi, 2001.
2. Kapoor, S.K., Human rights under International Law and Indian Law, Prentice Hall of India, New Delhi, 2002.
3. Basu, D.D., Indian Constitution, Oxford University Press, New Delhi, 2002.
4. Frankena, W.K., Ethics, Prentice Hall of India, New Delhi, 1990.
5. Meron Theodor, Human Rights and International Law Legal Policy Issues, Vol. 1 and 2, Ox ford University Press, New Delhi, 2000.

604103	Environmental Studies	Group I
ELECTIVE- III		
Teaching Scheme: **Lectures 3 Hrs/ Week**		**Examination Scheme:** **Theory:50 Marks (In Semester)** **50 Marks (End Semester)** **Credits 3**

Module I:

Introduction and Natural Resources: Multidisciplinary nature and public awareness, Renewable and nonrenewal resources and associated problems, Forest resources, Water resources, Mineral resources, Food resources, Energy resources, Land resources, Conservation of natural resources and human role.
Ecosystems: Concept, Structure and function, Producers composers and decomposers, Energy flow, Ecological succession, Food chains webs and ecological pyramids, Characteristics structures and functions of ecosystems such as Forest, Grassland, Desert, Aquatic ecosystems.

Module II

Environmental Pollution- Definition, Causes, effects and control of air pollution, water pollution, soil pollution, marine pollution, noise pollution, thermal pollution, nuclear hazards, human role in prevention of pollution, Solid waste management, Disaster management, floods, earthquake, cyclone and landslides.

Module III:

Social issues and Environment- Unsustainable to sustainable development, Urban problems related to energy, Water conservation and watershed management, Resettlement and re-habitation, Ethics, Climate change, Global warming, Acid rain, Ozone layer depletion, Nuclear accidents, holocaust, Waste land reclamation, Consumerism and waste products, Environment protection act, Wildlife protection act, Forest conservation act, Environmental issues in legislation, population explosion and family welfare program, Environment and human health, HIV, Women and child welfare, Role of information technology in
environment and human health.

References:

1. Agarwal, K.C., Environmental Biology, Nidi Publication Ltd., Bikaner, 2001.
2. Bharucha Erach, Biodiversity of India, Mapin Publishing Pvt. Ltd., Ahmadabad, 2002.
3.Bukhootsow, B., Energy Policy and Planning, Prentice Hall of India, New Delhi, 2003.
4.Cunningham, W.P., et al. , Environmental Encyclopedia, Jaico Publishing House, Mumbai, 2003.

604103	Energy Studies	Group I

ELECTIVE- III

Teaching Scheme: Lectures 3 Hrs/ Week		Examination Scheme: Theory : 50 Marks (In Semester) 50 Marks (End Semester) Credits : 3

Module I:

Energy Sources : Fossil fuels, Nuclear fuels, hydel, solar, wind and bio fuels in India, Energy conservation, Nuclear energy through fission and fusion processes.

Module II:

Energy Conservation: Energy conversion from source to utility, Solar, Nuclear, Geothermal, Tide and Wind Energies.

Global Energy Scenario: Role of energy in economic development and social transformation, Overall energy demand, availability and consumption, Depletion of energy resources and its impact on economy, Non proliferation of nuclear energy. International energy policies of G-8, G-20, OPEC and European union countries.

Module III:

Indian Energy Scenario- Commercial and noncommercial forms of energy, Utilization pattern in the past, present and also future prediction, Sector wise energy consumption.

Energy Policy: Energy policy issues at global level, national level and state level, Energy conservation act 2001, Electricity act 2003, Energy pricing and its impact on global variations

References:

1. Jose Goldenberg, Thomas Johanson, and Reddy, A.K.N., Energy for Sustainable World, WileyEastern ,2005.
2. Charles E. Brown, World Energy Resources, Springer Publication, New York, 2002.
3. Culp, A.W., Principles of Energy Conversion, McGraw Hill New York, 2004.
4. Bukhootsow, B., Energy Policy and Planning, Prentice Hall of India, New Delhi, 2003.

604103	Disaster Management	Group I
ELECTIVE- III		
Teaching Scheme: **Lectures 3 Hrs/ Week**		**Examination Scheme:** **Theory : 50 Marks (In Semester)** **50 Marks (End Semester)** **Credits : 3**

Module I

Introduction :Concepts and definitions: disaster, hazard, vulnerability, risk, capacity, impact, prevention, mitigation). Disasters classification; natural disasters (floods, draught, cyclones, volcanoes, earthquakes, tsunami, landslides, coastal erosion, soil erosion, forest fires etc.); manmade disasters (industrial pollution, artificial flooding in urban areas, nuclear radiation, chemical spills etc); hazard and vulnerability profile of India, mountain and coastal areas, ecological fragility

Module II

Disaster Impacts :Disaster impacts (environmental, physical, social, ecological, economical, political, etc.); health, psycho-social issues; demographic aspects (gender, age, special needs); hazard locations; global and national disaster trends; climate-change and urban disasters.

Module III

Disaster Risk Reduction (DRR) : Disaster management cycle – its phases; prevention, mitigation, preparedness, relief and recovery; structural and non-structural measures; risk analysis, vulnerability and capacity assessment; early warning systems, Post-disaster environmental response (water, sanitation, food safety, waste management, disease control); Roles and responsibilities of government, community, local institutions, NGOs and other stakeholders; Policies and legislation for disaster risk reduction, DRR programmes in India and the activities of National Disaster Management Authority.

References:

1. http://ndma.gov.in/ (Home page of National Disaster Management Authority).
2. http://www.ndmindia.nic.in/ (National Disaster management in India, Ministry of Home Affairs).
3. Pradeep Sahni, 2004, Disaster Risk Reduction in South Asia, Prentice Hall.
4. Singh B.K., 2008, Handbook of Disaster Management: techniques & Guidelines, Rajat Publication.
5. Ghosh G.K., 2006, Disaster Management ,APH Publishing Corporation.

604103	Knowledge Management	Group I
ELECTIVE- III		
Teaching Scheme: **Lectures 3 Hrs/ Week**		**Examination Scheme:** **Theory : 50 Marks (In Semester)** **50 Marks (End Semester)** **Credits : 3**

Module I

Introduction: Definition, evolution, need, drivers, scope, approaches in Organizations, strategies in organizations, components and functions, understanding knowledge; Learning organization: five components of learning organization, knowledge sources, and documentation. Essentials of Knowledge Management; knowledge creation process, knowledge management techniques, systems and tools.

Module II

Organizational knowledge management; architecture and implementation strategies, building the knowledge corporation and implementing knowledge management in organization. Knowledge management system life cycle, managing knowledge workers, knowledge audit, and knowledge management practices in organizations, few case studies

Module III

Futuristic KM: Knowledge Engineering, Theory of Computation, Data Structure.

References:

1. Knowledge Management – a resource book – A Thohothathri Raman, Excel, 2004.
2. Knowledge Management- Elias M. Awad Hasan M. Ghazri, Pearson Education
3. The KM Toolkit – Orchestrating IT, Strategy & Knowledge Platforms, Amrit Tiwana, Pearson, PHI, II Edn.
4. The Fifth Discipline Field Book – Strategies & Tools For Building A learning oganization PeterSenge et al. Nicholas Brealey 1994
5. Knowledge Management – Sudhir Warier, Vikas publications
6. Leading with Knowledge, Madanmohan Rao, Tata Mc-Graw Hill.

604103	Foreign Language	Group I
ELECTIVE- III		
Teaching Scheme: **Lectures 3 Hrs/ Week**		**Examination Scheme:** **Theory : 50 Marks (In Semester)** **50 Marks (End Semester)** **Credits : 3**
Module I:		
Pronunciation guidelines; Single vowels, Accentuated vowels, Vowels and consonants combinations, Consonants; Numbers 1-10 Articles and Genders; Gender in French, Plural articles, Some usual expressions. Pronouns and Verbs; The verb groups, The pronouns, Present tense, Some color Adjectives and Plural ; Adjectives, Some adjectives, Our first sentences, More Numbers.		
Module II:		
Sentences Structures; Some Prepositions, Normal Sentences, Negative Sentences, Interrogative Sentences, Exercises The Family; Vocabulary ,Conversation, Notes on Pronunciation, Notes on Vocabulary, Grammar, Liaisons Guideline. D'où viens-tu (Where do you come from); Vocabulary, Conversation, Notes on Vocabulary, Liaisons Guidelines . Comparer (Comparing); Vocabulary, Conversation, Notes on Vocabulary, Grammar Liaisons Guidelines, Ordinal Numbers		
Module III:		
Le temps (Time); Vocabulary, Grammar, Time on the clock Additional French Vocabulary; Vocabulary related to - The Family, Vocabulary related to - Where do you come from? French Expressions and Idioms; Day-to-day Life, At Work, The car, Sports, Specia Events Other French Flavours; Nos cousins d'Amérique - Québec et Accadie, Au pays de la bière et des frites, Mettez-vous à l'heure Suisse, Vé, peuchère, le français bien de chez nous		
Reference: http://www.jump-gate.com/languages/french/index.html		

604103	Engineering Economics	Group I
ELECTIVE- III		
Teaching Scheme: **Lectures 3 Hrs/ Week**		**Examination Scheme:** **Theory : 50 Marks (In Semester)** **50 Marks (End Semester)** **Credits : 3**

Module I:

Introduction to the subject: Micro and Macro Economics, Relationship between Science, Engineering, Technology and Economic Development. Production Possibility Curve, Nature of Economic Law, **Time Value of Money:** concepts and application. Capital budgeting; Traditional and modern methods, Payback period method, IRR, ARR, NPV, PI (with the help of case studies)

Module II:

Meaning of Production and factors of production, Law of variable proportions and returns to scale. Internal and external economies and diseconomies of scale. Concepts of cost of production, different types of costs; accounting cost, sunk cost, marginal cost, Opportunity cost. Break even analysis, Make or Buy decision (case study). Relevance of Depreciation towards industry. Meaning of market, types of market, perfect competition, Monopoly, Monopolistic, Oligopoly. (Main features). Supply and law of supply, Role of demand and supply in price determination.

Module III:

Indian Economy, nature and characteristics. Basic concepts; fiscal and monetary policy, LPG, Inflation, Sensex, GATT, WTO and IMF. Difference between Central bank and Commercial banks

Text Books:

1. Jain T.R., Economics for Engineers, VK Publication
2. Singh Seema, Economics for Engineers, IK International

Reference Books:

1. Chopra P. N., Principle of Economics, Kalyani Publishers
2. Dewett K. K., Modern economic theory, S. Chand
3. H. L. Ahuja., Modern economic theory, S. Chand
4. Dutt Rudar & Sundhram K. P. M., Indian Economy
5. Mishra S. K., Modern Micro Economics, Pragati Publications
6. Pandey I.M., Financial Management; Vikas Publishing House
7. Gupta Shashi K., Management Accounting, Kalyani Publication

604103	Engineering Risk – Benefit Analysis	Group I
ELECTIVE- III		
Teaching Scheme: **Lectures 3 Hrs/ Week**		**Examination Scheme:** **Theory : 50 Marks (In Semester)** **50 Marks (End Semester)** **Credits : 3**

Module I :

Introduction- Knowledge and Ignorance, Information Uncertainty in Engineering Systems, Introduction and overview of class; definition of Engineering risk; overview of Engineering risk analysis. Risk Methods: Risk Terminology, Risk Assessment, Risk Management and Control, Risk Acceptance, Risk Communication, Identifying and structuring the Engineering risk problem; developing a deterministic or parametric model System Definition and Structure: System Definition Models, Hierarchical Definitions of Systems, and System Complexity.

Module 2:

Reliability Assessment: Analytical Reliability Assessment, Empirical Reliability Analysis Using Life Data, Reliability Analysis of Systems

Module 3:

Reliability and probabilistic risk assessment (RPRA), decision analysis (DA), and cost-benefit analysis (CBA). All of these pertain to decision making in the presence of significant uncertainty. In ERBA, the issues of interest are: The risks associated with large engineering projects such as nuclear power reactors, the International Space Station, and critical infrastructures; the development of new products; the design of processes and operations with environmental externalities; and infrastructure renewal projects

Books:

1. Risk Analysis in Engineering and Economics, B. M. Ayyub, Chapman-Hall/CRC Press, 2003.
2. Hoyland, Arnljot, and Rausand, Marvin. *System Reliability Theory*. Hoboken, NJ: Wiley-Interscience, 1994. ISBN: 9780471471332.
3. Clemen, Robert, " Making Hard Decisions: An Introduction to Decision Analysis (Business Statistics) " PHI publications

604103	Optimization Techniques	Group II
ELECTIVE- III		
Teaching Scheme: **Lectures 2 Hrs/ Week**		**Examination Scheme:** **Theory : 50 Marks (In Semester)** **50 Marks (End Semester)** **Credits : 2**

Module I :

First and second order conditions for local interior optima (concavity and uniqueness), Sufficient conditions for unique global optima; Constrained optimization with Lagrange multipliers; Sufficient conditions for optima with equality and inequality constraints;

Module 2:

Recognizing and solving convex optimization problems. Convex sets, functions, and optimization problems. Least-squares, linear, and quadratic optimization. Geometric and semidefinite programming. Vector optimization. Duality theory. Convex relaxations. Approximation, fitting, and statistical estimation. Geometric problems. Control and trajectory planning

Books:

1. Stephen Boyd and Lieven Vandenberghe, *Convex Optimization*, Cambridge University Press.
2. A. Ben-Tal, A. Nemirovski, *Lectures on Modern Convex Optimization: Analysis,Algorithms, and Engineering Applications*, SIAM.
3. D. P. Bertsekas, A. Nedic, A. E. Ozdaglar, *Convex Analysis and Optimization*,Athena Scientific.
4. D. P. Bertsekas, *Nonlinear Programming*, Athena Scientific.
5. Y. Nesterov, *Introductory Lectures on Convex Optimization: A Basic Course*, Springer.
6. J. Borwein and A. S. Lewis, *Convex Analysis and Nonlinear Optimization:Theory and Examples*, Springer**.**

604103	Fuzzy Mathematics	Group II
ELECTIVE- III		
Teaching Scheme: **Lectures 2 Hrs/ Week**		**Examination Scheme:** **Theory : 50 Marks (In Semester)** **50 Marks (End Semester)** **Credits : 2**
Module I :		
Definition of a Fuzzy set; Elements of Fuzzy logic. Relations including, Operations, reflexivity, symmetry and transitivity; Pattern Classification based on fuzzy relations		
Module II:		
Fuzzy Models: Mamdani , Sugeno, Tsukamoto		
Books: 1. Neuro-Fuzzy and Soft Computing by S.R.Jung, Sun, Mizutani,		

604103	Design and Analysis of Algorithm	Group II
ELECTIVE- III		
Teaching Scheme: **Lectures 2 Hrs/ Week**		**Examination Scheme:** **Theory :** **50 Marks (In Semester)** **50 Marks (End Semester)** **Credits : 2**
Module I :		
Introduction- Fundamental characteristics of an algorithm. Basic algorithm analysis –Asymptotic analysis of complexity bounds– best, average and worst-case behaviour, standard notations for expressing algorithmic complexity. Empirical measurements of performance, time and space trade-offs in algorithms.		
Module II:		
Properties of big-Oh notation – Recurrence equations – Solving recurrence equations – Analysis of linear search. Divide and Conquer: General Method – Binary Search – Finding Maximum and Minimum – Merge Sort – Greedy Algorithms: General Method – Container Loading – Knapsack		
Books: Algorithm Design – Jon Kleinberg and Eva Tardos Introduction to Algorithms – T.H. Corman et. Al		

604103	CUDA	Group II
ELECTIVE- III		
Teaching Scheme: **Lectures 2 Hrs/ Week**		**Examination Scheme:** **Theory : 50 Marks (In Semester)** **50 Marks (End Semester)** **Credits : 2**
Module I :		
History of GPUs leading to their use and design for HPC- The Age of Parallel Processing, The Rise of GPU Computing ,CUDA, Applications of CUDA, Development Environment, Introduction to CUDA C, Kernel call, Passing Parameters, Querying Devices, Using Device Properties		
Module II:		
Parallel Programming in CUDA C - CUDA Parallel Programming, Splitting Parallel Blocks, Shared Memory and Synchronization, Constant Memory, Texture Memory, CUDA events, Measuring Performance with Events.		
Books: 1. Programming Massively Parallel Processors: A Hands-on Approach –second edition by David B. Kirk, Wen-mei W. Hwu. 2. CUDA by Example - An Introduction to General-Purpose GPU Programming by Jason Sanders ,Edward Kandrot- Addison Wesley 3. GPU Computing Gems Emerald Edition -Applications of GPU Computing Series by Wen-mei, W. Hwu 4. CUDA Programming: A Developer's Guide to Parallel Computing with GPUs by shane cook		

SEMESTER-IV

604206	Seminar III	
Teaching Scheme: **Practical 5 Hrs/ Week**		**Examination Scheme:** **Term Work : 50 Marks** **Oral/ Presentation: 50 Marks** **Credits :5**
Seminar III: shall preferably an extension of **seminar II.** The student shall submit the duly certified seminar report in standard format, for satisfactory completion of the work by the concerned guide and head of the Department/Institute.		

604207	Project Stage- II	
Teaching Scheme: **Practical 20 Hrs/ Week**		**Examination Scheme:** **Term Work : 200 Marks** **Oral/ Presentation: 100 Marks** **Credits :20**
Project Stage – II In Project Stage – II, the student shall complete the remaining part of the project which will consist of the fabrication of set up required for the project, work station, conducting experiments and taking results, analysis & validation of results and conclusions. The student shall prepare the duly certified final report of project work in standard format for satisfactory completion of the work by the concerned guide and head of the Department/Institute.		